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Analysis of Different Routing Algorithm for 2D-Torus Topology NoC Architecture under Load Variation

Bhupendra Kumar Soni[1], Dr.Girish Parmar[2]

[1]Department of Electronics and Communication Mewar University Chittorgarh, India
[2]Department of Electronics Engg. Rajasthan Technical University Kota, India

Abstract— *The recital of Network-on-Chip (NoC) depends on the underlying routing techniques. There are a lot of requirements that has to be met. Such performance metrics are minimum latency, least power and maximum throughput. This paper deals with XY route, PROM routing, FTXY routing and DyAD routing on 5x5 2D torus topology. The simulation is performed on nirgam NoC simulator version 2.1 for constant bit rate traffic condition. The simulation results reveals the dominance of XY, PROM, FTXY and DyAD algorithms depicting the minimum values of overall average latency per channel (in clock cycles per flit) as 0.409836 overall average latency per channel (in clock cycles per packet) as 6.2535, average throughput as 16.68, and total network power as 35.6768 mw, achieved for FTXY routing algorithm.*

Keywords— DyAD routing algorithm, Nirgam, NoC, 2D Torus topology, XY routing algorithm.

I. INTRODUCTION

Network on Chip (NoC) is a new model for System on Chip (SoC) design. The network consists of wires and routers. Processors, memories and other IP-blocks (Intellectual Property) are linked to routers. A routing algorithm acting a major role on network's function. Routers make the routing decisions based on the routing algorithm. The function of routing algorithm is to establish how the data is routed from sender to receiver. Topology defines how nodes are associated. Many different topologies like mesh, torus, mixed and custom topology. Some researchers have anticipated the application-specific topology that can offer better performance while minimizing area and energy consumption.The most common topologies are 2D mesh and torus. Mesh topology is easy to put into practice as all nodes are in equally distance and makes addressing of the cores quite simple during routing. In torus topology the corner and border nodes are horizontally and vertically connected our algorithm defines the best shortest route between source and destination. The rest of this paper is prearranged as follows. In section 2, we discuss literature review, section 3 the XY, PROM, FTXY and DyAD algorithms. Section 4 Architecture of 2D 5X5 Torus Topology NOC. Section 5 performance parameters of NoC. The results and graphs are discussed in section 6 and concluded in Section 7 presents the concluding remarks. The rest of this paper is organized as follows. In section 2, we discuss literature review, section 3 the XY, PROM, FTXY and DyAD algorithms. Section 4 Architecture of 2D 5X5 Torus Topology NOC. Section 5 performance parameters of NoC. The results and graphs are discussed in section 6 and concluded in Section 7 presents the concluding remarks.

II. LITERATURE REVIEW

Authors have proposed many routing algorithms and implemented these routing strategies on both regular and irregular NOC topologies. But the most common and well known type of routing algorithm is XY also known as dimension order routing. Amin Mehranzadeh , Mehdi Hoodgar [1] have proposed Fault Aware Routing Algorithm Based On XY Algorithm for Network on Chip , the effectiveness of FAXY by comparing it with XY routing schemes under different traffic patterns. Rajesh Nema, Parvinder Singh Khanna[2] have proposed in his paper Implementation of Two Phase X-Y Routing in NOC Router. Shubhangi D Chawade , Mahendraa Gaikwad [3] have proposed Reviewof XY Routing Algorithm for Network on chip Architecture. Dinesh Lekariya , Dr. M. A. Gaikwad [5] have proposed Performance Analysis of Minimum Hop Source Routing Algorithm for Two Dimensional Torus Topology NOC Architecture under CBR Traffic. Parag Parandkar , Jayesh kumar Dalal and Sumant Katiyal [6] have proposed Performance Comparison of XY, OE and DY Ad Routing Algorithm by Load Variation Analysis of 2-D Mesh Topology Based Network-on-Chip.Sudhanshu Choudhary Shafi Qureshi[7] have projected Performance Evaluation of Mesh-based NoCs realization of a New Architecture and Routing Algorithm. Naveen Choudhary

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M. S. Gaur V. Laxmi [8] have proposed Escape Path based Irregular Network-on-chip Simulation Framework. Haibo Zhu , Partha Pratim Pande , Cristian Grecu [10] have been proposed Performance Evaluation of Adaptive Routing Algorithms for achieving Fault Tolerance in NoC Fabrics. All these NOC models with a combination of different topologies and routing algorithms with different parameters have been simulated and tested using different simulators.

III. XY, PROM, FTXY AND DYAD ALGORITHMS

Routing Algorithm set up selection of path between source and destination switches chosen for transportation of packet. The routing algorithms are designed to achieve minimum communication latency, high throughput, and avoid starvations, deadlocks and live locks.

3.1 XY algorithms: This is one kind of disseminated deterministic routing algorithms. In which they used 2-Dimesion mesh topology and router which identified by its coordinate (x, y). The XY routing algorithm compares the present router address (Cx, Cy) to the destination router address (Dx, Dy) of the packet, stored in header flit. Flits routed to the core port of the router when the (Cx, Cy) address of the current router is equal to the (Dx, Dy) address. If this is not the case, the Dx address is firstly compared to the Cx (horizontal) address. Flits will be routed to the East port when Cx<Dx, to West when Cx>Dx and if Cx=Dx the header flit is previously horizontally aligned. If this last condition is true, the Dy (vertical) address is compared to the Cy address. Flits will be routed to South when CY<Dy, to North when CY>Dy.

3.2 PROM algorithms: The PROM algorithm uses only 2 virtual channels for deadlock-free routing which depends on the comparative position of the source node S and destination node D, and is the same for all flows traveling from source to destination:

1. If D lies to the east of S, vertical links use the first VC;
2. If D lies to the west of S, vertical links use the second VC;
3. If D lies directly north or South of S, both VCs are used;
4. All horizontal links may use all VCs.

3.3 FTXY algorithms: This algorithm offers fault tolerance and load matching traffic to pass up network congestion. FTXY is based on the principle of distance-vector routing in which each router notify their neighbors about its routing information. The selection of the path depends on routing table maintained by switches and network load. Routing table contain cost of reach destination in terms of hop counts. If there is network congestion the packet may follow different path.

3.4 DyAD algorithms: DyAD algorithm Network on Chip system uses vigorously both deterministic and adaptive routing algorithms to route packets. In vital situation when there are no congestions in the network the deterministic XY routing algorithm is used. Furthermore, when the network becomes congested the router switches to adaptive mode and uses the minimal odd-even routing. Each router in the DyAD network has a congestion flag, which tells that the router is congested. A router sends its flag to all its neighbor routers wherein the mode controller receives it and turns router to the adaptive mode when necessary. The advances of the DyAD are low latency in congestion free network but still good throughput in congestion network.

IV. ARCHITECTURE OF 2D 5X5 TORUS TOPOLOGY NOC

The routing Algorithm is simulated based on a 2-Dimension 5X5 torus topology NoC. Each tile consists of an IP core connected to a router by a bidirectional core channel. A tile is connected to neighbor tiles by four bidirectional channels (N, E, S and W). Each tile is identified by a unique integer ID. Also, each tile can be identified by a pair x-coordinate and y- coordinate. Our 2-Dimesion 5X5 torus topology NoC is designed using switching mechanism, in which packets are divided into flits. A packet consists of 3 types of flits, which are head flit, data flit and tail flit. All the four routing algorithms, XY routing algorithm, PROM routing algorithm, FTXY routing algorithm and DyAD routing algorithms are based on these characteristics.

V. PERFORMANCE PARAMETER

Some parameters that are used in evaluating the performance of NoCs are defined in this sub-section briefly.

Latency: It presents the required time to transfer n bytes of payload from its source to its destination. It consists of routing delay, argument delay, channel occupancy and overhead.

Bandwidth: It is the amount of data that can be moved using a communication link in a unit time period.

Throughput: It is the total number of received packets by the destinations per time unit.

Packet Loss: It happens when one or more packets do not reach their destination due to the error introduced by the network, the argument for network link or lack of buffer space etc.

Power-Performance Factor (φf): For most proficient routing scheme, low power consumption, smaller delays and high values of throughput are popular. To take all these factors into account, we define a figure of merit,

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power-performance factor derived from average value of performance metrics – power, latency, and throughput.

$$\text{Of} = \frac{(\text{Average power consumed} * \text{Average latency})}{\text{Average throughput}}$$

A low value of φf indicates low average power consumption, low latency and high average throughput. Lower the value of φf , better is performance of algorithm in terms of performance metrics.

VI. EXPERIMENTAL ANALYSIS

Simulation Results and Analysis: NIRGAM is a discrete event, cycle accurate simulator design for Network on Chip (NoC) research. This Simulator works in LINUX operating system. It sustain to experiment with NoC design in terms of routing algorithms and various topologies. NIRGAM is an extensible and modular system C based simulator. It allows the user to examine the performance (Average latency, throughput and total network power) of a NoC design. At present XY, PROM, DyAD and FTXY algorithms are simulated in NIRGAM. A set of parameters viz., packet size, generated traffic and traffic load were fixed for the simulations. The platform under concern composed of 5 × 5 array of tiles is interconnected by a 2D torus network .In this paper, XY, PROM ,FTXY and DyAD routing algorithms are considered and the results are analyzed. Tiles are attached to constant bit rate (CBR) traffic generator. The packet size is of 20 bytes with random destination mode. The percentage load, maximum bandwidth to be utilized, is varied beginning with 20 % to 100 % in the steps of 20 %. The interval between two successive flits is 2 clock cycles. Simulation runs for 50000 clock cycles and the clock frequency is 1 GHz. Performance Comparison of XY, PROM ,FTXY and DyAD Routing Algorithm by Load Variation Analysis of 2- Dimensional Torus Topology Based Network-on-Chip in the first 3000 clock cycles with warm-up period of 5 clock cycles.There are two measures of Performance of routing algorithms namely, overall average latency & total network power. The overall average latency in clock cycles per flit is also measured on a per channel basis on clock cycles per flit and clock cycles per packet. Total network power is measured in the units of mw.

In NIRGAM simulator % of Load (% of maximum bandwidth utilized) is varied and according to that the effect on performance parameters (Average Latency, Average Throughput and Total Network Power) is observed for warm-up time and total simulation time 5000 clock cycles. In this experiment % of Load is varied from 20% to 100% and in Table 1, 2 and 3 shows the simulation results of average latency (in clock cycle per packet), average throughput (in Gbps) and total network power (in mW) respectively for XY, PROM ,FTXY and DyAD routing algorithms for CBR (Constant Bit Rate) traffic generator . Figure 1, 2 shows the histograms of Table 2 and 3 respectively.

Table.1: Simulation results for load variation verses overall average latency per channel (in clock cycles per flit) for XY, PROM, FTXY and DyAD routing algorithms

Overall Average Latency per channel (in clock cycles per flit)				
% of Load	XY	PROM	FTXY	DYAD
20	1.04	1.05598	0.409836	0.865922
40	1.00358	1.33405	1.1674	1.02762
60	1.34169	2.19898	0.753521	1.41421
80	1.12724	1.47325	0.781046	0.778846
100	2.23574	1.1791	1.91	1.40476

Table.2: Simulation Data results for load variation verses overall average latency per channel (in clock cycles per packet) for XY, PROM, FTXY and DyAD routing algorithms

Overall Average Latency per channel (in clock cycles per Packet)				
% of Load	XY	PROM	FTXY	DYAD
20	10.4	7.49315	6.25	9.11765
40	9.3333	9.65891	8.27329	9.07317
60	8.67568	16.5769	8.23077	9.16854
80	8.30189	8.97219	7.96667	7.2
100	20.2759	11.2857	17.3636	11.8

Table.3: shows Percentage Load variation vs Total Network Power for XY, PROM, FTXY and DyAD routing algorithm

Total Network Power(in Mili Watt)				
% of Load	XY	PROM	FTXY	DYAD
20	38.8576	44.0684	35.6768	38.4139
40	44.641	48.7997	45.5868	41.7603
60	43.3273	58.9877	39.9662	46.4499
80	44.6347	64.6688	42.5767	41.22
100	42.4977	37.4132	42.091	39.5455

Performance metrics is the ratio between average throughput and average latency. More the “P” betters the Routing Algorithm.

P = Performance Metrics (Per channel basis)

$$= \frac{\text{Average Throughput}}{\text{Average Latency}}$$

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For XY Routing (100% Load) P = (9.92574/20.2759) = 0.489533
For PROM Routing (100% Load) P = (2.9475/11.2857) = 0.261171
For FTXY Routing (100% Load) P = (6.88/17.3636) = 0.3962312
For DyAD Routing (100% Load) P = (14.91/11.8) = 1.26355

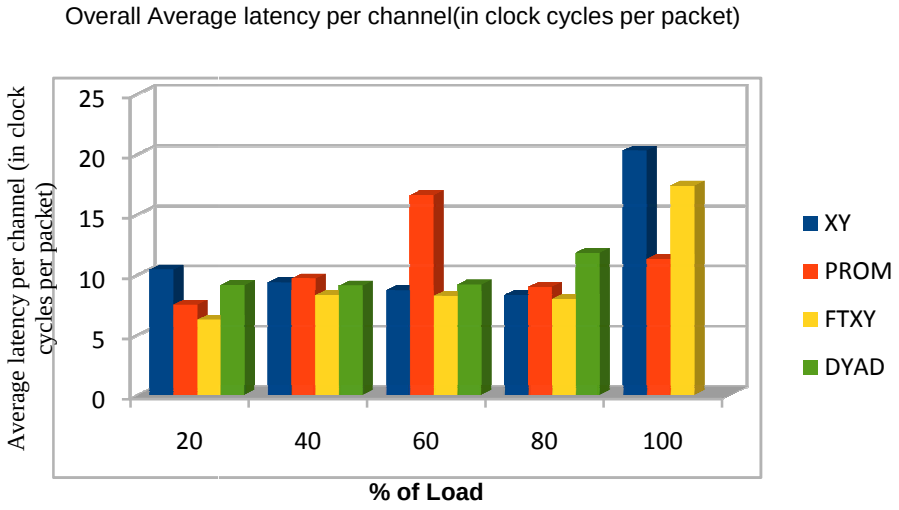

Fig.1: Graph of Percentage Load variation vs. overall average latency per channel (in clock cycles per packet) for XY, PROM, FTXY and DyAD routing algorithm

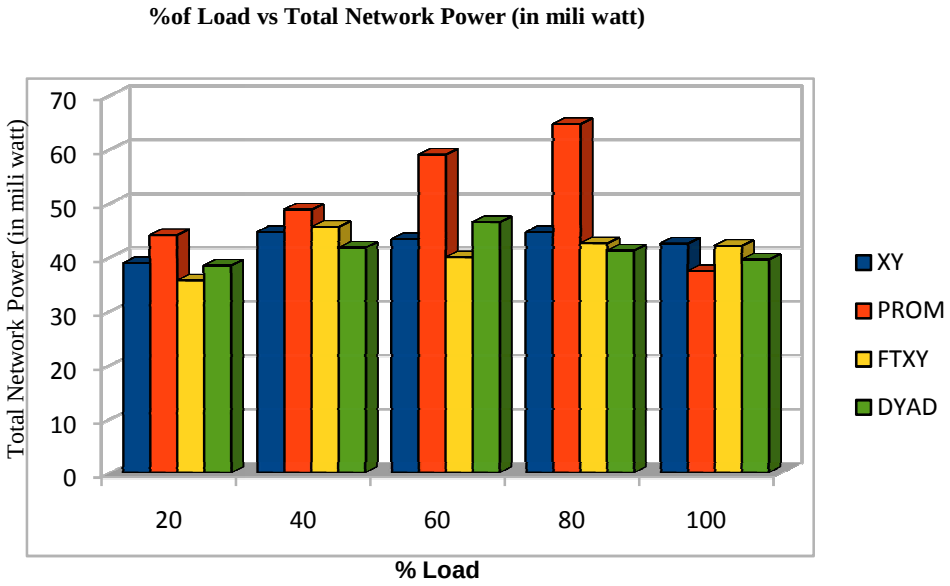

Fig.2: Graph of Percentage Load variation vs Total Network power (in milliwatts) for XY, PROM, FTXY and DyAD routing algorithm

The experimental setups for the evaluation of the routing algorithms are 5x5 torus topology where each node is connected with CBR (Constant Bit Rate) traffic generator of value 12 Gbps. Buffer depth (number of buffers) of input channel FIFO is 32. Number of virtual channels per physical channel is 5. Packet size is taken as 20 bytes with flit interval 2 clock cycles and clock frequency 1 Ghz. The Figure.3 is the power consumption graph under S and N channels in 5 × 5 torus based NoC topology. The Figure.3, 4 shows the power consumption graph and Throughput gaph for XY routing algorithm in Nirgam simulator. The Figure.5, 6 shows the power consumption graph and Throughput graph for PROM routing algorithm in Nirgam simulator. The Figure.7, 8 shows the power consumption graph and Throughput graph for FTXY routing algorithm in Nirgam simulator. The Figure.9, 10 shows the power consumption graph and Throughput graph for DyAD routing algorithm in Nirgam simulator.

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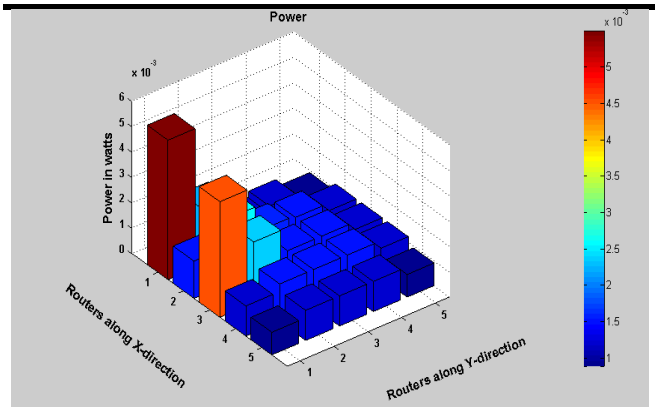

Fig.3: Power Consumption Graph for XY Routing Algorithm

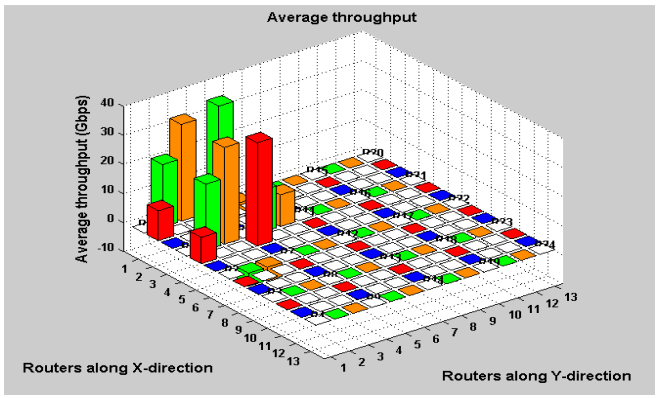

Fig.4: Throughput Graph for PROM Routing Algorithm

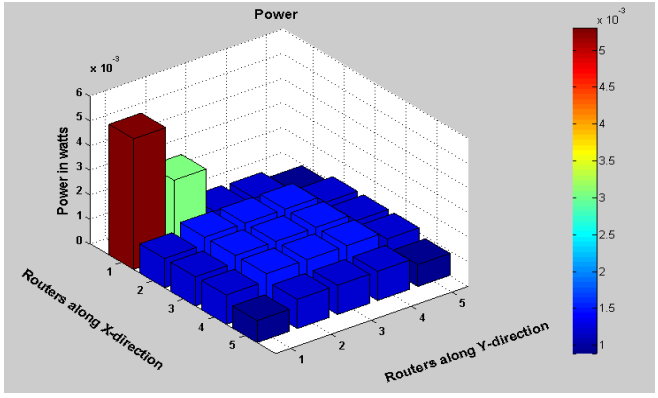

Fig.5: Power Consumption graph for PROM routing algorithm

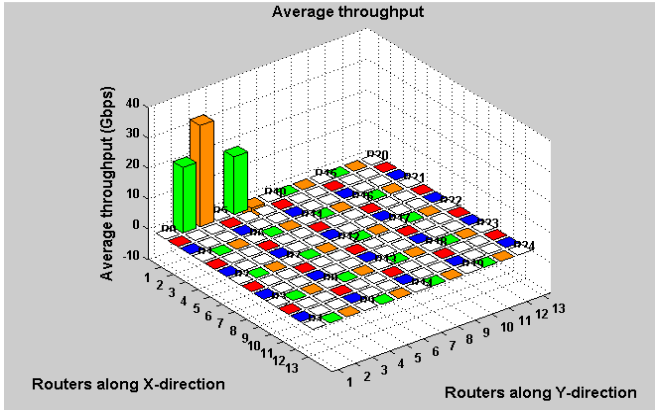

Fig.6: Throughput Graph for PROM Routing Algorithm

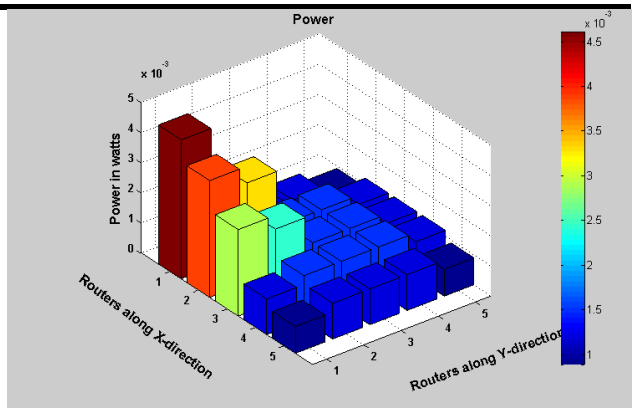

Fig.7: Power Consumption Graph for FTXY Routing Algorithm

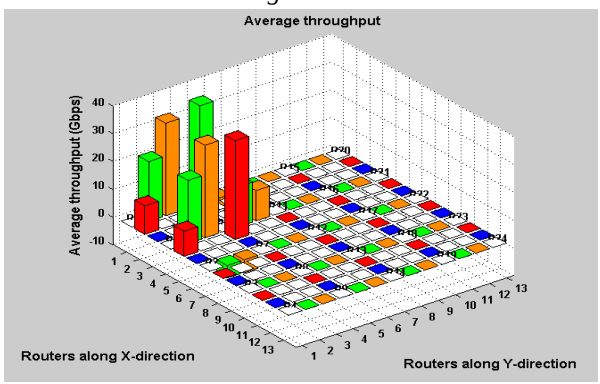

Fig.8: Throughput Graph for FTXY Routing Algorithm

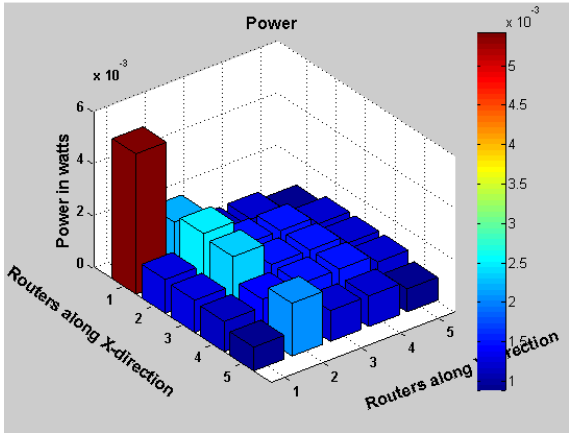

Fig.9: power consumption graph for DyAD routing algorithm

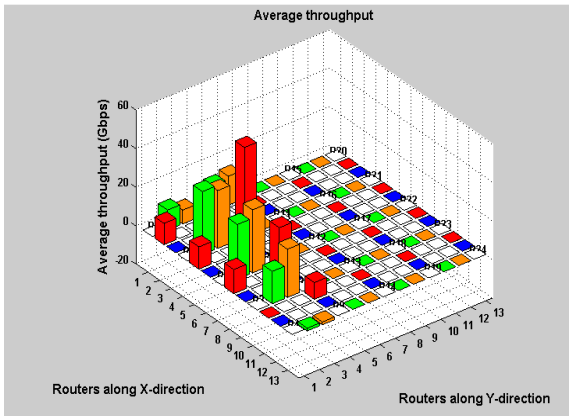

Fig.10: Throughput graph for DyAD routing algorithm

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From the above outcome and argument we are concluding that latency is in order of FTXY routing < DyAD routing < PROM routing < XY routing. FTXY routing algorithm is more efficient than other algorithms in Constant Bit Rate traffic pattern. Power efficiency of FTXY is more than DyAD routing. Throughput is in order of PROM routing < DyAD routing < FTXY routing < XY routing.

VII. CONCLUSION

The four versions of routing algorithms (XY, PROM, DyAD, and FTXY) are compared using 5 × 5 torus based technology with a clock rate of 1GHz. Performance estimation and comparison is done by varying % of maximum bandwidth utilized and routing algorithms. The simulation outcome shows that FTXY routing support low latency and low power in Constant Bit Rate traffic pattern. XY routing shows an marvelous throughput performance at Constant Bit Rate traffic pattern. The minimum value of overall average latency per channel (in clock cycles per flit) is obtained as 0.409836, overall average latency per channel (in clock cycles per packet) is obtained as 6.25, and total network power is obtained as 35.6768 milli watts, achieved for FTXY routing algorithm. Hence it is accomplished that the FTXY routing algorithm is very well suited for 5 × 5 torus topology.

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